REMARKS

Claims 1-12 remain pending in the application. Claims 1 has been amended without introduction of new matter. Support for this amendment may be found, for example, in Figure 30 and in the description on pages 29 and 30.

Claims 1, 2, 3, 5, and 12 stand rejected under 35 U.S.C. §102 (b) as allegedly being anticipated by each of Japanese Patent Number JP 08147163 ("Takemoto") and U.S. Patent Nos. 5,325,495 ("McLellan") and 5,555,384 ("Roberts"). Claims 4 and 6-8 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Takemoto in view of U.S. Patent No. 5,627,976 ("McFarland"). Claim 9 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Takemoto in view of U.S. Patent No. 5,128,926 ("Perlman"). Claims 10 and 11 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Takemoto in view of U.S. Patent No. 5,925,118 ("Revilla"). Favorable consideration is respectfully requested in view of the above amendments and the following remarks.

Exemplary embodiments describe a pipeline bus architecture that is specifically designed to transfer data from any one module to any other module in an arbitrary manner (Specification, p. 1, lines 7-16, and p. 15, line to p. 16, line 20). The modules perform functions on data transferred along the pipeline bus between modules connected to the bus. The transmitting module is typically enabled by an arbiter to take control of the bus while the module is putting data onto the bus.

In the cited documents, each of the "modules" **indicated by the Examiner** (referred to as registers) is constantly connected in the processor pipeline which performs processing on the data passing along that line. The bus in exemplary embodiments does not perform processing

operations on data being transferred along the pipeline bus; all the data processing is performed in the modules.

Based on the available English language abstract and Figure 1, Takemoto appears to disclose a pipeline including first and second data processing stages 13, 14 that perform prescribed instructions on data in the pipeline. The data to be processed is held in registers 15, 17, 19 that are connected in a by-pass path running parallel to the pipeline. Multiplexers 16, 18 and 20 select between the pipeline and the associated by-pass path in response to a controller 21. The registers of Takemoto are connected in parallel with the main data path of the pipeline and the registers, whether by-passed or not by-passed, are always connected between processing stages.

According to the Office Action, "registers" are equated to "modules" of claim 1. Takemoto differs from exemplary embodiments as claimed. Takemoto is directed to reducing the overall power consumption of a processing pipeline by the use of registers and by-pass paths, which are activated in response to specific operating parameters. Takemoto does not address whether or not the pipeline characteristics are affected by the connection or the by-passing of any one or more of the registers. In contrast, applicant's pipelined bus architecture employs the multiplexers to connect modules selectively to the pipeline. Applicant's solution enables the line characteristics to be preserved in the manner discussed in the Specification (p. 29, line 31 to p. 30, line 9).

The modules in exemplary embodiments are more complex than mere registers. A typical module is described at page 1, lines 11-13. Modules involve data processing of one degree or another and even a memory module would include more data handling facilities than a mere register, whose only function in Takemoto is to buffer or delay data. Exemplary

embodiments operate at a higher hierarchical level than Takemoto and are designed to provide a mechanism for connecting devices (modules) to a pipeline bus, as and when authorized such as, for example, when instructed by an arbiter. The bus connection unit that performs the connection enables a module to communicate with another via the bus and is the only means by which the module connects with the bus.

McLellan is directed to preventing stalling when the processor executes a branch instruction which is a problem associated with processor pipelines. This is irrelevant to exemplary embodiments because it is a bus and therefore is only used for data transfer. Branches, or any other instruction execution, do not occur on or affect a bus. However, the Office Action has indicated that it is the registers of the Q stages that are considered to be equivalent to the modules of the claims. Multiplexers 18 switch the data path to downstream stages between the through path or the Q-path. Contrary to assertions in the Office Action (¶ 10) that McLellan (at col. 4, lines 38-44) also discloses optimizing the signal characteristics, no such description is found in McLellan (in column 4 or in any other portion).

Therefore, it is respectfully submitted that McLellan does not actually disclose optimizing the signal characteristics. McLellan is not concerned with connecting modules of the level of complexity contemplated in exemplary embodiments to a pipeline bus architecture for the same reasons as apply to Takemoto.

The Office Action appears to confuse the issues of avoiding stalls and/or bubbles in the pipeline with electrical 'signal conditioning' in exemplary embodiments (i.e. accommodating and/or compensating for delays, slew rates and so on). By definition, a communication bus has to cover a 'large' distance in order to connect 'large' and widely spaced modules. On the other hand, a pipelined processor is designed to be compact with closely spaced pipeline stages,

virtually immediately adjacent, so there is no possibility for the problems of delays or issues relating to signal propagation to arise.

Roberts is similar to Takemoto and McLellan. As described in Roberts (col. 5, lines 42-51), by-pass multiplexers (referred to as element 30 but unmarked in Figure 6) are used to connect registers 33, 35, 37 in a pipeline. The multiplexers are used as in Takemoto to change the data path selectively from the preceding data processor/execution unit(s) or from the data I/O. Again, Roberts is not concerned with connecting high level modules to a pipelined bus in the same manner as encompassed in exemplary embodiments.

A common feature in each of Takemoto, McLellan and Roberts is that the multiplexers all select between a direct path and a by-pass path within a processor pipeline, as discussed above. As a result, one end of a register in the cited documents is always connected to the pipeline stage. In Takemoto, the output of one of the processors 13, 14 splits into two paths, a first path passes directly to the downstream multiplexer and a second path passes through a register in the by-pass path. The input side of the register is therefore constantly connected to the pipeline stage. Similarly, in McLellan, a Q-stage register 16, 16' is constantly connected to the output side of the preceding pipeline stage and lies in parallel to the direct path. The Q register is also always between two execution pipeline stages. Both the direct path and the by-pass path terminate at the downstream multiplexer. Furthermore, in Roberts, the units 33, 35 and the execution unit(s) are constantly connected in line with the pipeline through the multiplexers 30. In this case, however, it is the by-pass paths that are connected back to the I/O databus whereas the stages of the pipeline are permanently connected to the bus.

In each of Takemoto, McLellan and Roberts, data can only flow in one direction. Roberts is concerned with optimizing the operation of an execution pipeline in a computer,

where data and instructions would only flow in one direction. In all three documents, there is some form of data processing occurring in each stage of the bus. In Takemoto, there are data processing units 13, 14. In McLellan, the pipelined processing stages receive instructions from a parallel instruction line. Instructions for causing operations to be performed in the data path are input at 15 to each stage. In Roberts, the register pipeline contains execution unit(s) upstream of the registers 33, 34, 35.

In exemplary embodiments, however, the bus is purely for communication between modules and contains no processing facility. This is illustrated in Figure 3. Modules can only communicate via the pipeline bus and no processing is performed on data on the bus. Data from a selected module can be fed onto the bus and likewise data can be taken off the bus and fed to a selected module. As described (Specification, page 29, lines 25-30), only one of the modules is connected to the bus at any one time. In the cited documents, the processor modules (not to be confused with the registers as referred to in the Office Action) are permanently connected in series in the bus. The registers are always at least partially in series with the execution pipeline. The modules (as described on page 1, lines 11-13), are in fact more than merely registers, whose only function is to act as a delay or buffer. The bus enables the modules to transfer data between one another or to external devices (page 1, lines 16-18).

There is a difference between the organization of the modules and their connection with the bus (Specification, Figures 3 and 30). In exemplary embodiments, the modules can only transfer data between one another by being given access to/from the bus (in dependence on an arbitration unit) via the multiplexer of the bus connection unit. The modules in exemplary embodiments are only connected, and can only be connected, to the bus through the bus

connection units and the multiplexer circuitry within. The modules are not otherwise connected in the bus or to the bus, unlike the processor units of the cited documents.

Claim 1 has been amended to included the feature that "the modules are connected to the bus architecture only by way of the bus connection units and in response to operation of the multiplexer circuitry". This is not described in the cited documents as highlighted above. In the cited documents, at least one end of the registers equated by the Office Action with the "modules" of exemplary embodiments is always connected to the pipeline. The modules are only connected to the pipelined bus through operation of the multiplexers in the bus connection units. It is this facility that enables the bus connection unit to preserve/optimize the characteristics of the following line sections, whether or not a module is connected to the line or not. This facility would simply not be possible in any of the cited references.

In this regard, Applicants respectfully traverse assertions in the Office Action that in each case, the cited documents ensure optimization of the signal characteristics for the physical length of the bus portion concerned. The cited documents do not disclose (either explicitly or implicitly) this feature. Moreover, there is no reason for a person of average skill in the art to contemplate incorporating such a feature into any of the cited documents because each of the documents is concerned with a completely different technical subject to that described in exemplary embodiments. As mentioned above, the problems of signal optimization that can arise in a (communications) bus would simply not arise in any of the processor pipelines in the cited documents.

In order to make this distinction, claim 1 has been amended as recited above. First, it is now made clear that the plurality of modules are "adapted for selective connection" to the bus architecture. This is described and illustrated in Figure 30 and avoids any confusion as to

whether the modules are always "connected" to the bus or are "selectively" connected as has been argued above.

The paragraph stating with "each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture" has been moved to present a logical list of features.

Third, the paragraph stating how the modules are connected to the bus architecture has been expanded to explain that the modules are connected to the bus architecture only by way of the bus connection units and in response to operation of the multiplexer circuitry. Applicants respectfully submit that this wording specifies precisely, and in strict accordance with the corresponding description in pages 29 and 30, how a selected module is connected to the bus architecture.

It is respectfully submitted that amended claim 1 is not anticipated by any of the cited documents. It is further respectfully submitted that it would not be obvious to a person of average skill in the art to consider adding such a feature to any of the cited documents, not least because there would be no incentive to do so. Reconsideration of the rejections of claims is therefore, respectfully requested.

Claim 1 is, therefore, allowable over the cited documents. Claims 2-12, all of which depend on claim 1, are also allowable.

All of the rejections having been overcome, it is believed that this application is in condition for allowance and a notice to that effect is earnestly solicited. Should the Examiner have any questions with respect to expediting the prosecution of this application, she is urged to contact the undersigned at (703) 893-8500.

Respectfully submitted,
Potomac Patent Group PLLC

By: _____
Krishna Kalidindi
Registration No. 41,461

P.O. Box 270
Fredericksburg, Virginia 22404
703-893-8500

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